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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/882,480	06/14/2001	Hsiang-Lan Lung	15313.1	8120

7590 09/25/2002

KEVIN K. JOHANSON
WORKMAN NYDEGGER & SEELEY
1000 EAGLE GATE TOWER
60 EAST SOUTH TEMPLE
SALT LAKE CITY, UT 84111

EXAMINER
PIZARRO CRESPO, MARCOS D

ART UNIT	PAPER NUMBER
2814	6

DATE MAILED: 09/25/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/882,480	LUNG, HSIANG-LAN	
	Examiner	Art Unit	
	Marcos D. Pizarro-Crespo	2814	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 July 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-31* is/are pending in the application.

4a) Of the above claim(s) *11-21 and 26-31* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 22-25* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☒ Claim(s) *1-31* are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

Attorney's Docket Number: 15313.1
Filing Date: 6/14/2001
Claimed Foreign Priority Date: none
Applicant(s): Lung
Examiner: Marcos D. Pizarro-Crespo

DETAILED ACTION

This Office action responds to the election (paper no. 5) filed 7/8/2002.

Election/Restrictions

1. Claims 11-21 and 26-31 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected invention, there being no allowable generic or linking claim. Election was made **without** traverse in paper no. 5.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-10 and 24 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Line 24 of claim 1 recites the limitation "said gate oxide coating". There is insufficient antecedent basis for this limitation in the claim.

5. Lines 4-5 of claim 24 recite the limitation "said conducting polysilicon layer". There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

6. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Initially, and with respect to claims 5 and 6, note that "product by process" claims are directed to the product per se, no matter how actually made. See *In re Thorpe et al.*, 227 USPQ 964 (CAFC, 1985) and the related case law cited therein that makes it clear that it is the final product *per se* which must be determined in "product by process" claims, and not the patentability of the process, and that, as here, an old or obvious product produced by a new method is not patentable as a product, whether claimed in "product by process" claims or not. As stated in Thorpe,

> even though product-by-process claims are limited by and defined by the process, determination of patentability is based on the product itself. *In re Brown*, 459 F.2d 531, 535, 173 USPQ 685, 688 (CCPA 1972); *In re Pilkington*, 411 F.2d 1345, 1348, 162 USPQ 145, 147 (CCPA 1969); *Buono v. Yankee Maid Dress Corp.*, 77 F.2d 274, 279, 26 USPQ 57, 61 (2d. Cir. 1935).

Note that Applicant has burden of proof in such cases, as the above case law makes clear.

9. Claims 1 and 6-8 are rejected under 35 U.S.C. 102(b) as being anticipated by or, in the alternative, under 35 U.S.C. 103(a) as obvious over Onishi (US 5708284).

10. Onishi shows (see, *e.g.*, fig. 1) all aspects of the instant invention including a single transistor ferroelectric memory cell, comprising:

- a semiconductor substrate having defined thereon:
  - a first conductive-region **1** of a first conductivity-type (col.5/ll.57-62)
  - a source region **6c** of a second conductivity-type defined in the first conductive region **1** (col.5/ll.57-62)
  - a drain region **6a** of a second conductivity-type defined in the first conductive-region and spaced apart from the source region **6c** (col.5/ll.57-62)
  - a channel region comprising a portion of the first conductive-region **1** between the source region **6c** and the drain region **6a**
  - a gate oxide layer **2** on the semiconductor substrate covering the drain **6a**, channel, and source **6c** regions
- a ferroelectric gate unit disposed on the gate oxide layer **2**, the gate unit comprising:
  - a bottom electrode **8** in electrical communication with the drain region **6a**
  - a top electrode **10**
  - a ferroelectric layer **9** between the bottom **8** and the top **10** electrodes

- a sealing layer **7** on each side of the ferroelectric gate unit
- an upper conductive layer **11** on the ferroelectric gate unit and a portion of the gate oxide layer **2** such that the upper conductive layer **11** and the top electrode **10** of the ferroelectric gate unit are in electrical communication

wherein the source region **6c** is sized and configured to comprise a portion of the ferroelectric memory cell and an adjacent ferroelectric memory cell (see, *e.g.*, fig. 12).

11. Regarding claim 6, Onishi shows (col.5/ll.57-62) that the second conductivity-type source/drain regions include ions taken from the group consisting of P and As.

As to the grounds of rejection under section 103(a), the method step of implanting the ions, is an intermediate process step that does not affect the structure of the final device. See MPEP § 2113 which discusses the handling of "product by process" claims and recommends the alternative (§ 102 / § 103) grounds of rejection.

12. Regarding claim 7, Onishi shows that the bottom and top electrode may be composed of Pt, each having a thickness of about 500-1000 Å (col.6/ll.36,42-44,61-67).

13. Regarding claim 8, Onishi shows that the ferroelectric layer may be comprised of Pb(Zr, Ti)O3 having a thickness of 2000 Å (col.6/ll.55-61).

14. Claims 22-25 are rejected under 35 U.S.C. 102(b) as anticipated by Schlosser (WO 00/28596).

15. Schlosser shows (see, *e.g.*, fig. 2) all aspects of the instant invention including a ferroelectric memory cell comprising:

- a ferroelectric gate unit comprising a top electrode **KE2**, a layer of ferroelectric material **FS**, and a bottom electrode **KE1**

- a semiconductor substrate **1** having:
  - a drain **2**
  - a source **3**
  - a channel
  - a gate oxide **5**
- means for controlling the polarization of the layer of ferroelectric material **FS**

16. Regarding claim 23, Schlosser shows (see, *e.g.*, fig. 2) the means for controlling the polarization of the layer of ferroelectric material as an electrical connection between the drain **1** and the bottom electrode **KE1** of the ferroelectric gate unit.

17. Regarding claim 24, Schlosser shows (see, *e.g.*, fig. 2) the means for controlling the polarization of the layer of ferroelectric material as an upper polysilicon layer **11** deposited on top of the ferroelectric gate unit such that electrical communication is established between the top electrode **KE2** and the polysilicon layer **11**.

18. Regarding claim 25, Schlosser further shows (see, *e.g.*, fig. 2) the memory cell comprising a lower polysilicon layer **GS** deposited between the ferroelectric gate unit and the gate oxide **5**.

19. Claim 3 is rejected under 35 U.S.C. 103(a) as being unpatentable over Onishi in view of Chittipeddi (US 6294807) and Krivokapic (US 6100558).

20. Regarding claim 3, Onishi shows most aspects of the instant invention (see paragraphs 10-13 above), except for a plurality of isolation trenches defined in the semiconductor substrate.

Chittipeddi (col.4/ll.60-64), on the other hand, teaches that trench isolation structures are well known in the art for providing isolation between different devices on an integrated circuit substrate.

Moreover, Krivokapic (col.5/ll.13-16), teaches that trench isolation occupy less substrate surface-area than other currently known isolation techniques, *e.g.*, LOCOS.

It would have been obvious to a person having ordinary skill in the art at the time of the invention to have a plurality of isolation trenches defined in the substrate of Onishi, as suggested by Chittipeddi and Krivokapic, since they are conventionally used for isolation and will save space in the substrate, as opposed to other isolation techniques.

21. Claim 1 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schlosser in view of Fujiwara (US 5798548) and Koo (US 5959879).

22. Schlosser shows (see, *e.g.*, fig. 2) most aspects of the instant invention including a single transistor ferroelectric memory cell comprising:

- a semiconductor substrate having defined thereon:
  - a first conductive region **1**
  - source/drain regions **2, 3** of a second conductivity type defined in the first conductive region **1** (pp.8/ll.34-37)
  - a channel region comprising a portion of the first conductive region **1** between the source/drain regions **2, 3**
  - a gate oxide layer **5** on the semiconductor substrate covering the channel, and the source/drain regions **2, 3**

- a ferroelectric gate unit disposed on the gate oxide layer **5**, the gate unit comprising:
  - a bottom electrode **KE1** in electrical communication with the drain region **3**
  - a top electrode **KE2**
  - a ferroelectric layer **FS** between the bottom **KE1** and the top **KE2** electrodes
  - a sealing layer **8** on each side of the ferroelectric gate unit
  - an upper conductive layer **11** on the ferroelectric gate unit and a portion of the gate oxide layer **5** such that the upper conductive layer **11** and the top electrode **KE2** of the ferroelectric gate unit are in electrical communication

Schlosser, however, fails to show the source region **2** configured and sized so as to comprise a portion of the ferroelectric memory cell and an adjacent ferroelectric memory cell.

Fujiwara (col.8/ll.17-22), on the other hand, teaches that to reduce the occupying area of each memory cell on a substrate, two adjacent memory cells should share their source region.

Consequently, it would have been obvious at the time of the invention to one of ordinary skill in the art at the time of the invention to configure Schlosser's source region as taught by Fujiwara to reduce the occupying area of the memory cells on the substrate.

In addition, Schlosser (pp.6/ll.6-9, pp.8/ll.33-37) describes that the first conductive region is made of a suitable semiconductor substrate, in particular, a

substrate that contains monocrystalline silicon, more in particular, a monocrystalline silicon wafer. Schlosser, however, fails to specify a first conductivity-type for the first conductive region.

Fujiwara (col.3/ll.60-65), on the other hand, teaches that a well region on a monocrystalline silicon film may replace a monocrystalline silicon substrate. These well regions are conductive region of a first conductivity type that may be electrically coupled to respective word lines and independently biased during reading and writing operations (col.8/ll.37-40,55-59; col.9/ll.7-13,25-30,50-67; col.10/ll.1-17,63-67; col.11/ll.1-25).

Koo (col.5/ll.15-18) further teaches that this ability to independently control the potential of the well-region bias enables the formation of memory arrays having high integration-level and improves the efficiency of the reading and writing operations.

It would have been obvious at the time of the invention to one of ordinary skill in the art to have Schlosser's first conductive region to be of a first conductivity-type, as suggested by Fujiwara, in view of Koo, to improve the efficiency of the reading and writing operations of the cell.

23. Regarding claim 2, Schlosser shows (pp.10/ll.1) that the upper conductive layer comprises doped polysilicon.

24. Regarding claim 4, Schlosser shows (pp.9/ll.5-7) the memory cell further comprising a lower polysilicon layer **GS** between the gate oxide layer **5** and the bottom electrode **KE1**, the lower polysilicon layer **GS** doped to a conductive state.

Schlosser (pp.9/ll.7), however, shows that the thickness of the lower polysilicon layer may be as low as 1000-Å, instead of the claimed range of 500-700 Å.

Nonetheless, 700-Å is closed enough to 1000-Å that one of ordinary skill in the art would have expected Schlosser's polysilicon layer to have the same properties if made having a thickness of 700-Å. *Titanium Metal Corp. of America v. Banner*, 778 F.2d 775, 227 USPQ 773 (Fed. Cir. 1985).

In addition, it would be an obvious matter of design choice to made the polysilicon layer of 700 Å instead of 1000 Å, since such a modification would have involved a mere change in the size of a component. A change in size is generally recognized as being within the level of ordinary skill in the art. *In re Rose*, 105 USPQ 237 (CCPA 1955).

25. Claim 5 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schlosser in view of Fujiwara and Koo, as applied to claim 1 above, further in view of Jaeger.

26. Regarding claim 5, Schlosser/Fujiwara/Koo shows most aspects of the instant invention (see paragraphs 22-24 above), except that the first conductive region of a first conductivity type includes B ions. Nonetheless, Fujiwara shows (see, e.g., fig. 4) that the first conductivity region is a well region **42** that is predominantly p-type and according to Jaeger (pp.79/ll.26) boron is the only commonly used p-type dopant.

Consequently, it would have been obvious to one of ordinary skill in the art that the p-type conductive region of Schlosser/Fujiwara/Koo should include boron ions, as taught by Jaeger, since boron is the only commonly used p-type dopant.

27. Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Schlosser in view of Fujiwara and Koo, as applied to claim 1 above, further in view of Ahn (US 6420742).

28. Regarding claim 9, Schlosser/Fujiwara/Koo shows most aspects of the instant invention (see paragraphs 22-24 above). In addition, Schlosser (pp.9/ll.26-27) shows that the sealing layer comprises silicon dioxide. Schlosser/Fujiwara/Koo, however, fails to show that the sealing layer is made of silicon nitride.

Ahn (col.8/ll.65-col.9/ll.3), on the other hand, teaches that silicon nitride may substitute silicon oxide as the material for the sealing layer of Schlosser/Fujiwara/Koo.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to made the sealing layer of Schlosser/Fujiwara/Koo out of silicon nitride instead of silicon oxide, as it is suggested by Ahn, since either silicon nitride or silicon oxide may be used as materials for a sealing layer and the selection of any of these equivalent materials is within the level of ordinary skill in the art.

29. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Onishi in view of Schmidt (US 6172392).

30. Regarding claim 10, Onishi shows most aspects of the instant invention (see paragraphs 10-13 above), but fails to specify a channel length of 0.18 to 0.35 μm.

Schmidt (col.1/ll.16-23), on the other hand, teaches that the semiconductor processing-technology has progressively moved toward defining smaller features, characterized by transistors with a channel length of 0.18 microns. As feature size shrinks, the density of the resulting circuit increases.

Consequently, it would have been obvious to one of ordinary skill in the art at the time of the invention that the channel length of the memory cell of Onishi should have a channel of 0.18 microns, as taught by Schmidt, since channel lengths of 0.18 microns

are a characteristic of the current semiconductor technology that strives to increase circuit densities.

Conclusion

31. Papers related to this application may be submitted directly to Art Unit 2814 by facsimile transmission. Papers should be faxed to Art Unit 2814 via the Art Unit 2814 Fax Center located in Crystal Plaza 4, room 3C23. The faxing of such papers must conform to the notice published in the Official Gazette, 1096 OG 30 (15 November 1989). The Art Unit 2814 Fax Center number is **(703) 308-7722** or **–7724**. The Art Unit 2814 Fax Center is to be used only for papers related to Art Unit 2814 applications.

32. Any inquiry concerning this communication or earlier communications from the examiner should be directed to **Marcos D. Pizarro-Crespo** at **(703) 308-6558** and between the hours of 8:00 AM to 4:00 PM (Eastern Standard Time) Monday through Friday or by e-mail via Marcos.Pizarro@uspto.gov. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Olik Chaudhuri, can be reached on (703) 306-2794.

33. Any inquiry of a general nature or relating to the status of this application should be directed to the **Group 2800 Receptionist** at **(703) 308-0956**.

34. The following list is the Examiner's field of search for the present Office Action:

Field of Search	Date
U.S. Class / Subclass(es): 257/295,314-326,389; 438/3,279; 365/145	9/14/2002
Other Documentation: PLUS Analysis	9/14/2002
Electronic Database(s): EAST (USPAT, EPO, JPO, PGPub)	9/14/2002

Marcos D. Pizarro-Crespo
Patent Examiner
Art Unit 2814
703-308-6558
marcos.pizarro@uspto.gov

MDP/mdp
September 16, 2002

EDDIE LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800